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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,844	BALSDON ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 6/2/4, 8/23/4, 6/6/5, 6/22/5, 5/22/6
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/709,844 filed on 06/01/2004. Claims 1-20 remain pending in the application.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 18-20 are rejected under 35 U.S.C. 101 because

the claimed invention is directed to non-statutory subject matter. A computer program product stored on a computer readable storage medium for designing an integrated circuit is descriptive material and is nor statutory if not claimed as computer executable program, because without using the computer, just the stored program is not capable of causing the computer to design the integrated circuit.

4. Claims 18-20 are also rejected under 35 U.S.C. 112, first paragraph. Specifically, since the claimed invention is not supported by either a claims or Specification asserted utility or a well established utility for the reasons set forth above, one skilled in the art clearly would not know how to use the claimed invention.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section

351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-2, 5-11, 13-16 and 18-20 are rejected under 35 U.S.C. 102(e) as being unpatentable by Lin (US Pub. No.: 20060080630).

6. As to claims 1, 9, 13 and 18 Lin discloses:

(1) An electronic automation system comprising:

a shape-based database of an integrated circuit design (The floor plan design data may be created or stored in any conventional data format that will represent the desired floor plan design structures ... such as ... the "Open Access" database format – [0038]; The blocks of circuit elements then are arranged in the "core" area inside of the contact pads. With some blocks, the size and shape of the block are predefined – [0005]; ([0005]; [0006]; [0038]);

a mouse input device (The input devices 123 may include ... a pointing device such as a mouse ...- [0032], Fig.1);

a graphical user interface tool, capable of accessing and performing operations on the shape-based database, based on input from the mouse input device (the floor planning tool 201 allows a designer to easily position components of a microcircuit in a floor plan design, while maintaining desired attributes for the design. ... By using a pointing device, such as a keyboard, mouse, stylus, touchpad, joystick or the like, a circuit designer can select and move the placement of one or more of the blocks making up the floor plan design. As the designer moves a selected "target" block, the user interface graphically displays the various changes in the circuit characteristics and

design that will result from the movement of the target block - [0027], Fig.2) ([0027]; [0039]); and

an automatic router tool, capable of accessing the shape-based database, to create a interconnect route path for at least one net of the integrated circuit design, selected using the graphical user interface tool and the mouse (floor plan design tool 201, the circuit layout determination module 207 may employ a multi-step algorithm to automatically determine the routing of a wire network, such as a power/ground wire network. This algorithm may include, for example, (1) the construction of a visibility graph corresponding to the current arrangement of the floor plan design, (2) wire segment insertion into the design, (3) initial construction of the wire routing, and, (4) refinement of the wire routing - [0108], Fig.2), wherein the interconnect route path comprises segments having different interconnect widths (... if a channel box corresponds to a horizontal primary edge in the visibility graph, then a vertical wire segment is inserted into the channel box. Similarly, a horizontal wire segment for each needed power and ground network is inserted into each channel box corresponding to a vertical primary edge in the visibility graph. As discussed in detail above, the width of the inserted wire segment is calculated based upon the applicable attributes for that channel box - [0111]; If a wire's or via's determined current density value exceeds its specified maximum allowable current density value, then the PG wiring analysis module 1007 increases the width of the wire or via to correct this electromigration problem in step 1307- [0128]) ([0026]; [0027]; [0030]; [0035]; [0080]- [0083]; [0093]; [0094]; [0108]; [0111]; [0117]);

(9) A method of designing an integrated circuit comprising:

determining an interconnect route path between a first point and a second point of an integrated circuit design (a path between two blocks in the floor plan design is defined as an edge in the data structure describing the complete visibility graph ... empty space serves as a channel area or channel "box" through which connection wires, such as power/ground network wires, can be routed - [0072]);

comparing a property of the interconnect route path to a design rule (The PG wiring analysis module 1007 then compares the determined current density for each wire and via with the maximum current density allowable for the wire or via in step 1305 ... This maximum current density value allowable for each wire and via may be specified, for example, by the foundry that will be manufacturing integrated circuits from the design - [0127]);

if the property of the first interconnect path violates the design rule, creating an interconnect line for the interconnect route path having a first width (If a wire's or via's determined current density value exceeds its specified maximum allowable current density value, then the PG wiring analysis module 1007 increases the width of the wire or via to correct this electromigration problem in step 1307 - [0128]) ([0128]- [0131]; [0134]- [0137]); and

if the property of the first interconnect path meets the design rule, creating the interconnect line for the interconnect route path having a second width, different from the first width (Once the identified wiring problems in the received floor plan design 1201 have been corrected, or if the PG wiring analysis module 1007 determines that

there are no wiring problems in the received floor plan design 1201, then the floor plan design 1201 is provided to the area minimization module 1003. ... and then employs the well-known "Simplex" algorithm to determine the minimum suitable dimensions for each wire segment in the wiring of the received floor plan design 1201 - [0140]);

(13), (18) A method/program ([0035]) of designing an integrated circuit comprising:

determining an interconnect route path between a first point and a second point of an integrated (a path between two blocks in the floor plan design is defined as an edge in the data structure describing the complete visibility graph ... empty space serves as a channel area or channel "box" through which connection wires, such as power/ground network wires, can be routed - [0072]);

determining a property of the interconnect route path [0127]); and

creating an interconnect line for the interconnect route path having a width based on the property of the interconnect route path and a design rule ([0128]- [0131]; [00134]-[00137]).

7. As to claims 2, 5-8, 10-11, 14-16 and 19-20 Lin recites:

(2) The system further comprising a file, accessible by the automatic router tool, comprising a current density as a function of width ([0078]; [0128]- [0131]; [0139]);

(5) The system, wherein the automatic router tool uses at least one of Steiner tree algorithm ([0133]);

(6) The system further comprising a data import interface tool ([0033]);

(7) The system, wherein the integrated circuit design comprises at least one of a, digital, analog integrated circuit ([0103]- [0106]);

(8) The system, wherein automatic router tools creates interconnect route paths for two or more nets ([0111]);

(10), (11), (14), (19) The method/program, wherein the property is a current requirement of the interconnect route path ([0006]; [0127]);

(15), (16), (20) The method/program, wherein the determining an interconnect route path point between a first and a second point uses a gridless approach ([0005]; [0006]; [0038]; [0072]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable by Lin in view of Gentry et al. (US Patent 6,857,113).

With respect to claims 3 and 4 Lin teaches the features above but lacks an electronic automation system of an integrated circuit design further comprising frequency (clock speed/clock period) information for one or more nets.

9. As to claim 3 and 4 Gentry recites:

an electronic automation system of an integrated circuit design further comprising frequency (clock speed/clock period) information for one or more nets for assessing/judging electromigration risk of different nets based on frequency (clock speed/clock period) (col.2, ll.18-37; col.2, ll.54-64; col.4, ll.15-26; col.6, ll.43-53).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Gentry's teaching regarding the electronic automation system of an integrated circuit design further comprising frequency (clock speed/clock period) information for one or more nets and use it in Lin's invention to improve IC design by performing more accurate and reliable predictor of electromigration risk for high speed digital ICs when alternating current electromigration presents a higher risk to IC reliability.

10. Claims 12 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable by Lin in view of Tripathi et al. (US Patent 6,109,775).

With respect to claims 12 and 17 Lin teaches the features above but lacks an electronic automation method of an integrated circuit design, wherein a design rule is an optical proximity effect correction rule.

11. As to claim 12 and 17 Tripathi discloses:

an electronic automation method of an integrated circuit design using gridded approach, wherein a design rule is an optical proximity effect correction rule (col.3, ll.26-43; col.4, ll.42-46; col.4, ll.66-67; col.5, ll.1-10; col.13, ll.52-67; col.14, ll.1-11).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Tripathi teaching regarding the electronic automation

method of an integrated circuit design, wherein a design rule is an optical proximity effect correction rule and use in Lin's invention to improve a pattern design used in processing of integrated circuit structures.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

N L

THUAN DO
Primary examiner.
6/22/06